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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/035,747
Filing Date: December 28, 2001
Appellant(s): STEELE, GUY L.

Nathan A. Sloan
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 07, 2006 appealing from the Office action mailed May 31, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

The Appeal of U.S. Patent Application No. 10/035,579.

The Appeal of U.S. Patent Application No. 10/035,595.

The Appeal of U.S. Patent Application No. 10/035,584.

The Appeal of U.S. Patent Application No. 10/035,587.

The Appeal of U.S. Patent Application No. 10/035,647.

The Appeal of U.S. Patent Application No. 10/035,580.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-54.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The modifications are as follows:

Claims 1-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

It is noted that upon further review of the claims and the Huang et al. patent, it has been determined that Huang et al. anticipates the invention as recited in claims 6-20 and 32 currently under appeal, in addition to claims 1-5, 21-31 and 33-54 as set forth in the final action. The grounds of rejection section of this Examiner's Answer sets forth the modified rejection of claims 6-20 and 32 in view of Huang et al.

In addition, upon further review of the claims and the Lynch patent, it has been determined that Lynch et al. anticipates the invention as recited in claims 6-20 and 32 currently under appeal, in addition to claims 1-5, 21-31 and 33-54 as set forth in the final action. The grounds of rejection section of this Examiner's Answer sets forth the modified rejection of claims 6-20 and 32 in view of Lynch et al.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,995,991	HUANG ET AL.	11-1999
6,009,511	LYNCH ET AL.	12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

Claims 1-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch et al .

(10) Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

B. Claims 1-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al.

As per independent claims 1-4, Huang et al teach, e.g., see **Fig. 4**, the invention, **arithmetic calculation circuit (100)**, including: **X and Y operand registers 116 & 118; arithmetic section 114; memory (register file) 112**. Each operand register (X or Y) has a first portion (116-1, 118-1) and second portion (116-2, 118-2).

As per dependent claim 5, the claim recites the detail regarding "status". The second portion (e.g. 116-2, 118-2) in Huang's disclosed operand registers corresponds to this claimed feature.

Due to the similarity of claims 21-31 and 33-54 to claims 1-5, they are rejected under a similar rationale.

As per dependent claims 6-15, the claims add the detail "formats", "flags", "status". The claimed formats are inherent features in the floating point operands in Huang. The status and flags are disclosed in col. 1 lines 55-60, col. 7 lines 20-23 and table 1 in col. 6 of the Huang patent.

As per claims 16-20, the claims are similar to claims 1-15 except the independent claim 16 adds the "floating point operand data" having "sign", "exponent" and "fraction" information. Huang et al's device is a floating point device wherein the floating point operands includes sign, exponent and fraction information (res_sgn, res_exp and res_mag in Fig. 4, output of Arithmetic section).

As per dependent claim 32, the claim an "additional function-processing unit". Huang et al.s special operand generator 122 corresponds to the additional functional unit as claimed.

C. Claims 1-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch et al .

As per independent claims 1-4, Lynch et al teach, e.g., see **Fig. 4**, the invention, **floating point unit (36)**, including: **Register Stack (84) and FPU Core (94)**, **FPU Core (94)**, **FPU control (92)**, **Assembly Queue (80)**. The Register Stack (84) has a first portion (87) and second portion (89).

As per dependent claim 5, the claims add the detail regarding "status". Lynch's disclosed second portion of the operand (e.g. 89) corresponds to this claimed feature.

Due to the similarity of claims 21-31 and 33-54 to claims 1-5, they are rejected under a similar rationale.

As per dependent claims 6-15, the claims add the detail "formats", "flags", "status". These features are inherent in the special floating point number in Lynch (see e.g. Fig. 5).

As per claims 16-20, the claims are similar to claims 1-15 except the independent claim 16 adds the "floating point operand data" having "sign", "exponent" and "fraction" information. Lynch et al's device is a floating point device, therefore these features are inherent in the floating point operands in Lynch.

As per dependent claim 32, the claim adds an "additional function processing unit" Lynch discloses a Reorder Buffer corresponding to the claimed additional functional unit .

(11) Response to Argument

Appellant's arguments filed April 07, 2006 have been fully considered but they are not persuasive. Appellant argues that:

B1. Claims 1-5 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, "a floating point operand data structure" including "embedded status information associated with at least one status condition of the floating point operand data." Huang fails to teach or suggest this element."

B2. Claim 2 patentably distinguishes from Huang

Huang does not disclose each and every element of dependent claim 2. Dependent claim 2 recites determining 'at least one status condition' from 'the embedded status information without regard to memory storage external to the data structure' (emphasis added). The Examiner has not addressed any of the elements recited by dependent claim 2. See Office Action mailed November 15, 2004 at p. 2. These elements are not taught by Huang. In fact, as discussed above, Huang discloses the opposite of the claimed structure, teaching use of registers 116 and 118, which are memory storage external to the operand data structure (Huang, FIG. 4; col. 6, line 65). Accordingly, Huang cannot anticipate dependent claim 2. Appellant requests that the Board allow this claim."

B3. Claim 3 patentably distinguishes from Huang

"Huang does not disclose each and every element of dependent claim 3.

Dependent claim 3 recites '[t]he floating point operand data structure of claim 2, wherein the memory storage external to the data structure is a floating point status register.' As with claim 2, the Examiner has not addressed any of the elements recited by dependent claim 3. See Office Action mailed November 15, 2004 at p. 2. These elements are not taught by Huang. In fact, as discussed above, Huang discloses the opposite of the claimed structure, teaching use of registers 116 and 118 (Huang, FIG. 4; col. 6, line 65), which is the structure that claim 3 (as depending from claim 2) distinguishes. Accordingly, Huang cannot anticipate dependent claim 3. Appellant requests that the Board allow this claim."

B4. Claim 4 patentably distinguishes from Huang

"Huang does not disclose each and every element of dependent claim 4. Dependent claim 4 recites '[t]he enhanced floating point operand data structure of claim 3, wherein the outcome of a conditional floating point instruction is based on the embedded status information without regard to contents of the floating point status register' (emphasis added). Once again, the Examiner has not addressed any of the elements recited by dependent claim 4. See Office Action mailed November 15, 2004 at p. 2. These elements are not taught by Huang. In fact, as discussed above, Huang discloses the opposite of the claimed structure, teaching use of the contents of registers 116 and 118 (Huang, FIG. 4; col. 6, line 65). Accordingly, Huang cannot anticipate dependent claim 4. Appellant requests that the Board allow this claim."

B5. Claims 21-31 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed

invention. Independent claim 21 calls for a combination including, for example,

> an operand memory storage device for maintaining the floating point operand;
> a control unit in communication with the operand memory storage device, the control unit receiving at least one floating point instruction associated with the at least one floating point operation and generating at least one control signal related to the at least one floating point operation; and
> a first functional processing unit in communication with the operand memory storage device and the control unit, the first functional processing unit capable processing the floating point operand and storing status information within the processed floating point operand

(emphasis added). Unsurprisingly, the Examiner has yet again failed to address claim elements such as 'operand memory storage device,' 'control unit,' 'control signal,' and 'functional processing unit ... capable [of] ... storing status information within the processed floating point operand' See Office Action mailed November 15, 2004 at p. 3. Huang fails to teach at least these elements of claim 21.

Moreover, Huang does not teach or suggest a 'functional processing unit ... capable [of] ... storing status information within the processed floating point operand,' as recited by independent claim 21 (emphasis added). Even assuming that Huang's tag constitutes the claimed 'status information,' which Appellant does not concede, Huang illustrates in FIG. 4 a separate tag generator 150 and separate special operand generators 122. Such teachings do not constitute a teaching or suggestion of a 'functional processing unit ... capable [of] ... storing status information within the processed floating point operand,' as recited by independent claim 21. As discussed above regarding the rejection of claim 1, Huang does not teach or suggest 'storing status information within the processed floating point operand,' as recited by claim 21."

B6. Claims 23 and 29 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 23 and 29. Dependent claim 23 recites '[t]he floating point system of claim 21, wherein the first functional processing unit is capable of embedding the status information related to the processed floating point operand within predetermined fields of the processed floating point operand' (emphasis added). The Examiner has not addressed these elements. See Office Action mailed November 15, 2004 at p. 3. As discussed above, Huang merely teaches storing a tag in a separate tag portion 118-2 (Huang, FIG. 4; col. 6, line 66 through col. 7, line 2). Such a teaching by Huang constitutes neither the claimed 'embedding ... within ... the processed floating point operand,' nor the claimed 'embedding ... within predetermined fields of the processed floating point operand.' Dependent claim 29, although of different scope, recites similar elements to dependent claim 23. Accordingly, Huang cannot anticipate dependent claims 23 and 29. Appellant requests that the Board allow these claims."

B7. Claims 24 and 30 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 24 and 30. Dependent claim 24 recites '[t]he floating point system of claim 21, wherein the first functional processing unit is capable of providing the processed floating point operand to the operand memory storage device without storing the status information to a separate status memory device' (emphasis added). The Examiner has not addressed these elements. See Office Action mailed November 15, 2004 at p. 3. Indeed, Huang clearly illustrates using a separate memory storage device, tag generator 150, to

generate tag values which are stored in register 116-2 (Huang, FIG. 4; col. 7, lines 31-34). Such a teaching by Huang does not constitute the claimed "providing the processed floating point operand to the operand memory storage device without storing the status information to a separate status memory device" (emphasis added). Dependent claim 30, although of different scope, recites elements similar to dependent claim 24. Accordingly, Huang cannot anticipate dependent claims 24 and 30. Appellant requests that the Board allow these claims."

B8. Claims 25 and 31 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 25 and 31. Dependent claim 25 recites "[t]he floating point system of claim 24, wherein the control unit is operative to condition the outcome of the floating point instruction based upon the status information within the processed floating point operand without accessing the separate status memory device" (emphasis added). The Examiner has not addressed these elements, nor does Huang teach or suggest such elements. See Office Action mailed November 15, 2004 at p. 3. Dependent claim 31, although of different scope, recites elements similar to dependent claim 25. Accordingly, Huang cannot anticipate dependent claims 25 and 31. Appellant requests that the Board allow these claims."

B9. Claim 26 patentably distinguishes from Huang

"Huang does not disclose each and every element of dependent claim 26. Dependent claim 25 recites '[t]he floating point system of claim 21 further comprising a second functional processing unit in communication with the memory storage device

and the control unit, the second functional processing unit being capable of processing a second floating point operand and storing status information related to the second floating point operand while the status information related to the first floating point operand is preserved" (emphasis added). The Examiner has not addressed this element, nor does Huang teach or suggest such elements. See Office Action mailed November 15, 2004 at p. 3."

B10. Claims 33-39 and 44-50 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 33 recites

> A method of encoding a floating point operand with status information without maintaining the status information in a floating point status register, comprising:
> determining a status condition of the floating point operand as part of processing the floating point operand in association with a floating point operation; and
> representing an updated status condition of the floating point operand within the floating point operand

(emphasis added)...

Moreover, as discussed above regarding claim 1, Huang does not teach or suggest "representing an updated status condition of the floating point operand within the floating point operand," as recited by independent claim 33. Accordingly, Huang cannot anticipate this claim.

Further, Huang clearly does not teach or suggest 'encoding a floating point operand with status information without maintaining the status information in a floating point status register,' as recited by claim 33. Rather, Huang explicitly teaches use of operand registers 116 and 118 that maintain tag values (alleged status information) in a

separate portion 116-2 and 118-2. Such teachings do not constitute a teaching or suggest of 'encoding a floating point operand with status information without maintaining the status information in a floating point status register,' as recited by claim 33. For at least this additional reason, Huang cannot anticipate independent claim 33."

B11. Claims 40-43 and 51-54 patentably distinguish from Huang

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 40 recites

> A method of encoding a floating point operand with status information related to a status of the floating point operand without maintaining the status information in a floating point status register, comprising:
> receiving a floating point instruction;
> accessing a floating point operand to be processed as part of processing the floating point instruction;
> decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand; and
> encoding a resulting status condition from execution of the floating point instruction on the floating point operand as updated status information within the floating point operand

(emphasis added). As discussed above with respect to independent claim 33, Huang fails to teach at least 'encoding a floating point operand with status information related to a status of the floating point operand without maintaining the status information in a floating point status register' and 'encoding a resulting status condition ... within the floating point operand,' as recited by independent claim 40. Accordingly, Huang cannot anticipate independent claim 40.

Moreover, Huang does not teach or suggest 'decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand,' as recited by independent claim 40. Rather, as discussed above,

Huang receives "status conditions" from tag portion 116-2 (FIG. 4), which is separate from operand portion 116-1. Such teachings of Huang do not constitute a teaching or suggestion of 'decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand,' as recited by independent claim 40. Accordingly, for at least this additional reason, Huang cannot anticipate independent claim 40."

C1. Claims 1-5 patentably distinguish from Lynch

"Lynch does not disclose each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example, "a floating point operand data structure" including "embedded status information associated with at least one status condition of the floating point operand data." Lynch fails to teach or suggest this element."

C2. Claim 2 patentably distinguishes from Lynch

"Lynch does not disclose each and every element of dependent claim 2. Dependent claim 2 recites determining "at least one status condition" from "the embedded status information without regard to memory storage external to the data structure" (emphasis added). The Examiner has not addressed any of the elements recited by dependent claim 2. See Office Action mailed November 15, 2004 at p. 3. In fact, these elements are not taught by Lynch. Indeed, as discussed above, Lynch discloses the opposite of the claimed structure, teaching use of a Register Stack 84 including a separate Tag Field 89 (alleged status), which is memory storage external to

Lynch's Reg Field 87 (alleged operand) (Lynch, FIG. 4). Accordingly, Lynch cannot anticipate dependent claim 2. Appellant requests that the Board allow this claim."

C3. Claim 3 patentably distinguishes from Lynch

"Lynch does not disclose each and every element of dependent claim 3. Dependent claim 3 recites '[t]he floating point operand data structure of claim 2, wherein the memory storage external to the data structure is a floating point status register.' Once again, the Examiner has not addressed any of the elements recited by dependent claim 3. See Office Action mailed November 15, 2004 at p. 3. In fact, Lynch does not teach or suggest the elements of claim 3. Indeed, as discussed above, Lynch discloses the opposite of the claimed structure, teaching use of a Register Stack 84 including a separate Tag Field 89 (Lynch, FIG. 4). Accordingly, Lynch cannot anticipate dependent claim 3. Appellant requests that the Board allow this claim."

C4. Claim 4 patentably distinguishes from Lynch

"Lynch does not disclose each and every element of dependent claim 4. Dependent claim 4 recites '[t]he enhanced floating point operand data structure of claim 3, wherein the outcome of a conditional floating point instruction is based on the embedded status information without regard to contents of the floating point status register' (emphasis added). The Examiner has not addressed any of the elements recited by dependent claim 4. See Office Action mailed November 15, 2004 at p. 3. In fact, Lynch does not teach or suggest these elements. Indeed, as discussed above, Lynch teaches the opposite of the claimed structure, teaching use of a Register Stack

84 (Lynch, FIG. 4). Accordingly, Lynch cannot anticipate dependent claim 4. Appellant requests that the Board allow this claim."

C5. Claims 21-31 patentably distinguish from Lynch

"Lynch does not disclose each and every element of Appellant's claimed invention. Independent claim 21 calls for a combination including, for example,

> an operand memory storage device for maintaining the floating point operand;
> a control unit in communication with the operand memory storage device, the control unit receiving at least one floating point instruction associated with the at least one floating point operation and generating at least one control signal related to the at least one floating point operation; and
> a first functional processing unit in communication with the operand memory storage device and the control unit, the first functional processing unit capable processing the floating point operand and storing status information within the processed floating point operand

(emphasis added). The Examiner has not addressed how Lynch allegedly teaches or suggests the claimed 'operand memory storage device,' 'control unit,' 'control signal,' 'functional processing unit ... capable [of] ... storing status information within the processed floating point operand.' See Office Action mailed November 15, 2004 at p. 3. Lynch fails to teach at least these elements. Accordingly, Lynch cannot anticipate independent claim 21.

Moreover, Lynch does not teach or suggest a 'functional processing unit ... capable [of] ... storing status information within the processed floating point operand,' as recited by independent claim 21. Even assuming that Lynch's tag constitutes the claimed 'status information,' which Appellant does not concede, Lynch clearly illustrates in FIG. 4 a separate tag field 89 and a separate register field 87. Such teachings do not constitute a teaching or suggestion of a 'functional processing unit ... capable [of] ...

storing status information within the processed floating point operand,' as recited by independent claim 21. As discussed above regarding the rejection of claim 1 as allegedly anticipated by Lynch, Lynch does not teach or suggest 'storing status information within the processed floating point operand,' as recited by claim 21."

C6. Claims 23 and 29 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 23 and 29. Dependent claim 23 recites '[t]he floating point system of claim 21, wherein the first functional processing unit is capable of embedding the status information related to the processed floating point operand within predetermined fields of the processed floating point operand.' The Examiner has not addressed these elements. See Office Action mailed November 15, 2004 at p. 3. As discussed above, Lynch merely teaches storing a tag in a separate Tag Field 89 (Lynch, FIG. 4). Such a teaching by Lynch constitutes neither the claimed 'embedding ... within ... the processed floating point operand,' nor the claimed 'embedding ... within predetermined fields of the processed floating point operand.' Dependent claim 29, although of different scope, recites similar elements to dependent claim 23. Accordingly, Lynch cannot anticipate dependent claims 23 and 29. Appellant requests that the Board allow these claims."

C7. Claims 24 and 30 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 24 and 30. Dependent claim 24 recites '[t]he floating point system of claim 21, wherein the first functional processing unit is capable of providing the processed floating point operand to the operand memory storage device without storing the status information to a

separate status memory device' (emphasis added). The Examiner has not addressed these elements. See Office Action mailed November 15, 2004 at p. 3. In fact, Lynch does not teach or suggest the claimed elements. Indeed, as discussed above, Lynch discloses the opposite of the claimed structure, teaching use of a separate memory storage device, Tag Field 89 (Lynch, FIG. 4; col. 5, lines 44-45). Such a teaching by Lynch does not constitute the claimed 'providing the processed floating point operand to the operand memory storage device without storing the status information to a separate status memory device,' as recited by dependent claim 24 (emphasis added). Dependent claim 30, although of different scope, recites elements similar to dependent claim 24. Accordingly, Lynch cannot anticipate dependent claims 24 and 30. Appellant requests that the Board allow these claims."

C8. Claims 25 and 31 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 25 and 31. Dependent claim 25 recites '[t]he floating point system of claim 24, wherein the control unit is operative to condition the outcome of the floating point instruction based upon the status information within the processed floating point operand without accessing the separate status memory device' (emphasis added). The Examiner has not addressed these elements, nor does Lynch teach or suggest these elements. See Office Action mailed November 15, 2004 at p. 3. Dependent claim 31, although of different scope, recites elements similar to dependent claim 25. Accordingly, Lynch

cannot anticipate dependent claims 25 and 31. Appellant requests that the Board allow these claims."

C9. Claim 26 patentably distinguishes from Lynch

"Lynch does not disclose each and every element of dependent claim 26. Dependent claim 25 recites '[t]he floating point system of claim 21 further comprising a second functional processing unit in communication with the memory storage device and the control unit, the second functional processing unit being capable of processing a second floating point operand and storing status information related to the second floating point operand while the status information related to the first floating point operand is preserved,' as recited by dependent claim 26 (emphasis added). The Examiner has not addressed these elements, nor does Lynch teach or suggest these elements. See Office Action mailed November 15, 2004 at p. 3."

C10. Claims 33-39 and 44-50 patentably distinguish from Lynch

"Huang does not disclose each and every element of Appellant's claimed invention. Independent claim 33 recites

> A method of encoding a floating point operand with status information without maintaining the status information in a floating point status register, comprising:
> determining a status condition of the floating point operand as part of processing the floating point operand in association with a floating point operation; and
> representing an updated status condition of the floating point operand within the floating point operand

(emphasis added)...

Moreover, as discussed above regarding the rejection of claim 1 as anticipated

by Lynch, Lynch does not teach or suggest 'representing an updated status condition of the floating point operand within the floating point operand,' as recited by independent claim 33. Accordingly, Lynch cannot anticipate this claim.

Further, Lynch clearly does not teach or suggest "encoding a floating point operand with status information without maintaining the status information in a floating point status register," as recited by claim 33. Rather, Lynch explicitly teaches use of Register Stack 89 including a Tag Field 89 (storing alleged status information) separate from Reg Field 87 (storing alleged operand). Lynch, FIG. 4, col. 15, lines 63-67, col. 16, lines 11-13). Such teachings do not constitute a teaching or suggest of "encoding a floating point operand with status information without maintaining the status information in a floating point status register," as recited by claim 33. For at least this additional reason, Lynch cannot anticipate independent claim 33."

C11. Claims 40-43 and 51-54 patentably distinguish from Lynch

"Lynch does not disclose each and every element of Appellant's claimed invention. Independent claim 40 recites

> A method of encoding a floating point operand with status information related to a status of the floating point operand without maintaining the status information in a floating point status register, comprising:
> receiving a floating point instruction;
> accessing a floating point operand to be processed as part of processing the floating point instruction;
> decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand; and
> encoding a resulting status condition from execution of the floating point instruction on the floating point operand as updated status information within the floating point operand

(emphasis added). As discussed above with respect to independent claim 33, Lynch

fails to teach at least 'encoding a floating point operand with status information related to a status of the floating point operand without maintaining the status information in a floating point status register' and 'encoding a resulting status condition ... within the floating point operand,' as recited by independent claim 40. Accordingly, Lynch cannot anticipate independent claim 40.

Moreover, Huang does not teach or suggest 'decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand,' as recited by independent claim 40. Rather, as discussed above, Lynch allegedly receives 'status conditions' from Tag Field 89 (FIG. 4), which is separate from Reg. Field 87. Such teachings of Lynch do not constitute a teaching or suggestion of decoding an initial status condition of the floating point operand from only status information embedded within the floating point operand,' as recited by independent claim 40. Accordingly, for at least this additional reason, Lynch cannot anticipate independent claim 40."

D1. Claims 6-15 patentably distinguish from Huang

"Claims 6-15 depend from independent claim 1 and therefore include all of the elements recited therein. As discussed above, Huang does not teach each and every element of claim 1. Moreover, the Examiner has not addressed any of the elements of claims 6-15, other than to make a general conclusion that 'the features are well known' (Office Action mailed November 15, 2004 at p. 4). The Examiner has not provided any documentary evidence supporting these general conclusions, despite Appellant's request (Request for Reconsideration filed August 4, 2005 at pp. 14-15). Because the

Examiner has not set forth how Huang allegedly teaches or suggests each and every element, has not provided any other reference to cure Huang's deficiencies, and has not provided the requisite motivation to modify Huang to arrive at Appellant's claimed invention, no prima facie case of obviousness has been established with respect to claims 6-15. Appellant requests the Board to allow these claims."

D2. Claims 16-20 patentably distinguish from Huang

"No prima facie case of obviousness has been established with respect to independent claims 16-20 because Huang fails to teach or suggest each and every element recited by the claim and because there is no motivation to modify Huang to arrive at Appellant's claimed invention.

Independent claim 16 recites a combination including, for example,

> a first data field having sign information associated with the floating point operand;
> a second data field having exponent information associated with the floating point operand; and
> a third data field having fractional information associated with the floating point operand, wherein at least one of the first data field, the second data field and the third data field further includes embedded status information associated with at least one operand status condition.

The Examiner asserts that "the examiner believes that a 'floating point data' should have 'sign', 'exponent' and 'fraction' information'" (Office Action mailed June 6, 2005 at p. 4). As discussed above, the Examiner's 'belief' that Huang 'should have' the elements of claim 16 and that 'Huang et al's device is a floating point device' does not establish that Huang teaches each and every element of claim 16. The Examiner has not cited any portion of Huang as teaching or suggesting these claimed elements."

D3. Claims 17-18 patentably distinguish from Huang

"Huang does not disclose each and every element of dependent claims 17 and

18, nor is there any motivation to modify Huang to arrive at Appellant's claimed invention. As discussed above with regard to claims 3 and 4, the Examiner has not addressed any of the elements recited by dependent claims 17 and 18. See Office Action mailed November 15, 2004 at p. 4. Accordingly, no prima facie case of obviousness has been established for these claims. Appellant requests that the Board allow these claims."

D4. Claim 32 patentably distinguishes from Huang

"Huang does not disclose each and every element of dependent claim 32, nor is there any motivation to modify Huang to arrive at Appellant's claimed invention. Claim 32 recites

> The floating point system of claim 31 further comprising an additional functional processing unit in communication with the operand memory register and the control unit, the additional functional processing unit being capable of concurrently processing an additional floating point operand and storing status information related to the additional floating point operand within the additional floating point operand while the status information related to the other floating point operand is preserved within the other floating point operand

(emphasis added). The Examiner merely asserts "[t]he feature is obvious to a person having ordinary skill in the art." See Office Action mailed November 15, 2004 at p. 4. This bare assertion cannot establish that Huang teaches or suggests all elements recited by claim 32. Moreover, the Examiner has not provided any motivation to modify Huang to arrive at Appellant's claimed invention. Accordingly, no prima facie case of obviousness has been established for claim 32. Appellant requests that the Board allow claim 32."

E1. Claims 6-15 patentably distinguish from Lynch

"Claims 6-15 depend from independent claim 1 and therefore include all of the elements recited therein. As established above, Lynch fails to teach or suggest each and every element of claim 1. The Examiner does not cite any other references to curt the deficiencies of Lynch discussed above. Moreover, the Examiner has not addressed any of the elements of claims 6-15, other than to make a general conclusion that "the features are well known" (Office Action mailed November 15, 2004 at p. 4) and has failed to cite any documentary evidence supporting these general conclusions, despite Appellant's request (Request for Reconsideration filed August 4, 2005 at p. 21). Because the Examiner has not set forth how Lynch allegedly teaches or suggests each nd every element, has not provided any other reference to cure Lynch's deficiencies, a and has not provided the requisite motivation to modify Lynch to arrive at Appellant's claimed invention, no prima facie case of obviousness has been established with respect to claims 6-15. Appellant requests the Board to allow these claims."

E2. Claims 16-20 patentably distinguish from Lynch

"No prima facie case of obviousness has been established with respect to independent claims 16-20 because Lynch fails to teach or suggest each and every element recited by the claim and because there is no motivation to modify Lynch to arrive at Appellant's claimed invention.

Independent claim 16 recites a combination including, for example,

> a first data field having sign information associated with the floating point operand;
> a second data field having exponent information associated with the floating point operand; and
> a third data field having fractional information associated with the

> floating point operand, wherein at least one of the first data field, the second data field and the third data field further includes embedded status information associated with at least one operand status condition.

The Examiner asserts that "the examiner believes that a 'floating point data' should have 'sign', 'exponent' and 'fraction' information'" (Office Action mailed June 6, 2005 at p. 4). As discussed above, the Examiner's 'belief' that Lynch 'should have' the elements of claim 16 and that 'Lynch et al's device is a floating point device' does not establish that Huang teaches each and every element of claim 16. The Examiner has not cited any portion of Lynch as teaching or suggesting these claimed elements."

E3. Claims 17-18 and 20 patentably distinguish from Lynch

"Lynch does not disclose each and every element of dependent claims 17, 18, and 20, which are dependent from claim 16, nor is there any motivation to modify Lynch to arrive at Appellant's claimed invention. The Examiner has not addressed any of the elements recited by dependent claims 17, 18, and 20. See Office Action mailed November 15, 2004 at p. 4. Accordingly, no prima facie case of obviousness has been established for these claims. Appellant requests that the Board allow these claims."

E4. Claim 32 patentably distinguishes from Lynch

"Lynch does not disclose each and every element of dependent claim 32, nor is there any motivation to modify Lynch to arrive at Appellant's claimed invention. Claim 32 recites

> The floating point system of claim 31 further comprising an additional functional processing unit in communication with the operand memory register and the control unit, the additional functional processing unit being capable of concurrently processing an additional floating point operand and storing status information related to the additional floating point operand within the additional floating point operand while the status information related to the other floating point operand is preserved within

the other floating point operand

(emphasis added). The Examiner merely asserts "[t]he feature is obvious to a person having ordinary skill in the art." See Office Action mailed November 15, 2004 at p. 4. Once again, the Examiner's bare assertion cannot be substituted for the required teaching or suggestion in the prior art of the elements recited by claim 32, and the required motivation to modify Lynch to arrive at Appellant's claimed invention. Accordingly, no prima facie case of obviousness has been established for these claims. Appellant requests that the Board allow these claims."

With respect to the arguments, the examiner carefully reviews Appellant's specification, drawings, claimed invention and the applied references.

B1. Claims 1-5

According to Fig. 4, "X" (116-1) and "x_tag" 116-2 are belonged to a "X" register 116. In col. 6, lines 64-65, Huang specifically states "**X** and Y **operand** registers **116** and 118...". Therefore, it is clearl that Huang teaches the claimed "first portion", i.e., "X" (116-1) and "second portion ... having embedded status information associated with at least one status condition...", i.e., "x_tag" (116-2).

B2. Claim 2

Huang clearly teaches the feature, e.g., see Abstract, lines 5-10 "[i]n a second step, a tag associated with each of the operands is also stored in the same or different memory. Each of the tags has a tag value that indicates whether or not its associated operand represents an ordinary operand value or a special operand value"; TABLE 1;

and Claim 1, para. (a). Therefore, Huang's tag (x_tag) 166-1 is a portion of X operand register 116 as the claimed "at least one status condition is determined from the embedded status information without regard to memory storage external to the data structure".

B3-B4. Claims 3-4

It is noted that the phrase "without regard to memory storage external to the data structure" in parent claim [2] implied the embedded status information is not associated with data from the memory storage external like Appellant's Fig. 1 (PRIOR ART, FLOATING POINT STATUS REGISTER 25). Therefore, Huang's tag (x_tag) 166-1 is the same as the claimed features.

B5. Claims 21-31

Huang does disclose the claimed "operand memory storage device" (see element 112 "MEMORY (REGISTER FILE)"); and "first functional processing unit" (see elements 114 & 150 "ARITHMETIC SECTION & TAG GENERATOR") of independent claim 21. Although the tag generator (150) to generate the tag value separately from the output of arithmetic section (114), the examiner believes that the storing status information "tag value" within the processed floating point operand. It is noted that the format [storing status information within the processed floating point operand] of **stored data** in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transfered** to "X" operand register 116 because the **read out / write in data** is usually unchanged. It is noted that Huang does not disclose the claimed "control unit"; however, a system/device, e.g., Appellant's Fig.

1 (PRIOR ART), which uses Huang's floating point architecture should have such "control unit" as claimed.

B6. Claims 23 & 29

As discuss in paragraph **B5** above, the **stored** "processed floating point operand" [in the memory MEMORY (REGISTER FILE) 112] includes "status information".

B7. Claims 24 & 30

As discuss in paragraph **B5** above, the **stored** "processed floating point operand" [in the memory MEMORY (REGISTER FILE) 112] includes "status information".

B8. Claims 25 & 31

Because the **stored** "processed floating point operand" [in the memory MEMORY (REGISTER FILE) 112] includes "status information" and the **transferred** "processed floating point operand" to the X operand register 116, Huang's floating point architecture performs the same function as claimed.

B9. Claim 26

It is noted that Huang does not disclose the claimed "second functional processing unit"; however, a system/device, e.g., Appellant's Fig. 1 (PRIOR ART), which uses Huang's floating point architecture should have such "second functional processing unit" as claimed. It is noted that Huang's MEMORY (REGISTER FILES) 112 can read out / write in a plurality of operands. Therefore, Huang's MEMORY (REGISTER FILES) 112 preserves the stored data as claimed.

B10. Claims 33-39 & 44-50

Independent claim 33 recites a method corresponding to apparatus claims 2-4. See discussion in paragraphs **B2, B3 & B4** above.

B11. Claims 40-43 & 51-54

Independent claim 40 recites a method corresponding to apparatus claims 22-24. See discussion in paragraphs **B5, B6 & B7** above.

C1. Claims 1-5

It is noted that the "Tag Field" (89) contains the "status" information of each register of Register Stack (84), e.g., see Abstract. According to Fig. 4, "Reg Field" (87) and "Tag Field" (89) are belonged to Register Stack (84). Therefore, it is clearly that Lynch teaches the claimed "first portion", i.e., "Reg Field" (87) and "second portion ... having embedded status information associated with at least one status condition...", i.e., "Tag Field" (89).

C2. Claim 2

Lynch clearly teaches the feature, e.g., see Abstract, lines 5-7 "[a]dditionally, the tag value indicates the type of special floating point number"; Fig. 5. Therefore, Lynch's Tag Field 89 is a portion of Register Stack 84 as the claimed "at least one status condition is determined from the embedded status information without regard to memory storage external to the data structure".

C3-C4. Claims 3-4

It is noted that the phrase "without regard to memory storage external to the data

structure" in parent claim [2] implied the embedded status information is not associated with data from the memory storage external like Appellant's Fig. 1 (PRIOR ART, FLOATING POINT STATUS REGISTER 25). Therefore, Lynch's Tag Field 89 is the same as the claimed features.

C5. Claims 21-31

Lynch does disclose the claimed "operand memory storage device" (Register Stack 84); and "first functional processing unit" (FPU Core 94 & Result Queue 96) of independent claim 21. Although the tag value is appended to each floating point number stored in a floating point register, the examiner interprets the floating point register as a operand the examiner believes that the storing status information "tag Field" within the processed floating point operand. It is noted that Lynch does not disclose the claimed "control unit"; however, Lynch's microprocessor (Fig. 1) inherently includes such "control unit".

C6. Claims 23 & 29

As discuss in paragraph **C5** above, the **stored** "processed floating point operand" in the Register Stack 84 includes "status information".

C7. Claims 24 & 30

As discuss in paragraph **C5** above, the **stored** "processed floating point operand" in the Register Stack 84 includes "status information".

C8. Claims 25 & 31

Because the **stored** "processed floating point operand" in the Register Stack 84 includes "status information", Lynch's apparatus performs the same function as claimed.

C9. Claim 26

It is noted that Lynch does disclose the claimed "second functional processing unit" (e. g., see Fig.1, Functional Units 24A-24C). It is noted that Lynch's FPU 36 coupled to Register File 30. Therefore, Lynch's Register Stack 84 and Register File 30 preserve the stored data as claimed.

C10. Claims 33-39 & 44-50

Independent claim 33 recites a method corresponding to apparatus claims 2-4. See discussion in paragraphs **C2, C3 & C4** above.

C11. Claims 40-43 & 51-54

Independent claim 40 recites a method corresponding to apparatus claims 22-24. See discussion in paragraphs **C5, C6 & C7** above.

D1. Claims 6-15

As pointed out in this Examiners Answer, the examiner points out Huang's teaching of the "status" information, e.g., zero, overflow, underflow, etc. status flags (col. 7, lines 20-23); Not a number, etc. (TABLE 1).

D2. Claims 16-20

Independent claim 16 is similar to independent claim 1. The claim further adds the detail of "data fields", i.e., sign, exponent & fraction. These data fields are standard format of floating point operand, as pointed out in the rejection.

D3. Claims 17-18

Dependent claims 17-18 are similar to apparatus claims 2-4. See discussion in

paragraphs **B2, B3 & B4** above.

D4. Claim 32

Dependent claim 32 is similar to apparatus claims 26. See discussion in paragraph **B9** above.

E1. Claims 6-15

The rejection of claims 6-15 in this Examiner's Answer points out Lynch's teaching regarding "status" information, e.g.,"[t]ypes of special floating point numbers include zero, +infinity, -infinity and NaNs" (col. 17, lines 6-7) and Fig. 5.

E2. Claims 16-20

Independent claim 16 is similar to independent claim 1. The claim further adds the detail of "data fields", i.e., sign, exponent & fraction. These data fields are inherent and standard format of floating point operand.

E3. Claims 17-18 and 20

Dependent claims 17-18 and 20 are similar apparatus to claims 2-4. See discussion in paragraphs **C2, C3 & C4** above.

E4. Claim 32

Dependent claim 32 is similar to apparatus claims 26. See discussion in paragraph **C9** above.

(12) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(13) For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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